

S/N 10/716,953

Page 2

CISCO-8481

LISTING OF THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims on the application. Claims being amended are set forth in a larger font than all other claims. All claims are set forth below with one of the following annotations.

- (Original): Claim filed with the application following the specification.
- (Currently amended): Claim being amended in the current amendment paper.
- (Cancelled): Claim cancelled or deleted from the application.
- (Withdrawn): Claim still in the application, but in a non-elected status.
- (New): Claim being added in the current amendment paper.
- (Previously presented): Claim not being currently amended, but which was amended or was new in a previous amendment paper.
- (Not entered): Claim presented in a previous amendment, but not entered or whose entry status unknown. No claim text is shown.

1. (Currently Amended) A monolithic integrated circuit comprising:

a first subcircuit;

a second subcircuit; and

a bias current supply coupled to the first and second subcircuits ~~including~~
including:

a first bias circuit coupled to and to supply bias current to the first subcircuit, the first bias circuit including a first current modulator having a first switch input to control the rate of change of supplied bias current in response to the first switch input, the first switch input to indicate that the bias current is to start or stop being supplied to the first subcircuit, subcircuit; and

a second bias circuit coupled to and to supply bias current to the second subcircuit.

BEST AVAILABLE COPY

S/N 10/716,953

Page 3

CISCO-8481

2. (Currently Amended) An integrated circuit as described in claim 1, wherein the first and second subcircuits are to operate during mutually exclusive time periods.
3. (Original) A monolithic integrated circuit comprising:
 - a substrate;
 - a first set of one or more subcircuits on the substrate;
 - a second set of one or more subcircuits on the substrate; and
 - a bias current supply coupled to the first and second sets to provide bias current to the first and second sets, and including:
 - a first bias circuit on the substrate coupled to and to supply bias current to a first subcircuit of the first set, the first bias circuit including a first current modulator having a first switch input to control the rate of change of supplied bias current in response to the first switch input, the first switch input to indicate that the bias current is to start or stop being supplied to the first subcircuit.
4. (Original) An integrated circuit as described in claim 3, wherein the first and second sets of subcircuits are to operate during mutually exclusive time periods.
5. (Original) An integrated circuit as described in claim 3, wherein the first and second sets comprise metal oxide semiconductor transistors.
6. (Original) An integrated circuit as described in claim 5, wherein the first and second sets comprise metal oxide semiconductor transistors in a CMOS configuration.
- 7-23. (Cancelled)
24. (Original) A radio frequency (RF) monolithic integrated circuit comprising:
 - a first RF subcircuit;
 - a second RF subcircuit; and

BEST AVAILABLE COPY

S/N 10/716,953

Page 4

CISCO-8481

a bias current supply coupled to the first and second subcircuits including

a first bias circuit coupled to and to supply bias current to the first subcircuit, the first bias circuit including a first current modulator having a first switch input to control the rate of change of supplied bias current in response to the first switch input, the first switch input to indicate that the bias current is to start or stop being supplied to the first subcircuit, and

a second bias circuit coupled to and to supply bias current to the second subcircuit.

25. (Currently Amended) An integrated circuit as described in claim 24, wherein the first and second RF subcircuits are to operate during mutually exclusive time periods.

26. (Original) A monolithic radio frequency (RF) integrated circuit comprising:

a substrate;

a first set of one or more RF subcircuits on the substrate;

a second set of one or more RF subcircuits on the substrate; and

a bias current supply coupled to the first and second sets to provide bias current to the first and second sets, and including:

a first bias circuit on the substrate coupled to and to supply bias current to a first RF subcircuit of the first set, the first bias circuit including a first current modulator having a first switch input to control the rate of change of supplied bias current in response to the first switch input, the first switch input to indicate that the bias current is to start or stop being supplied to the first RF subcircuit.

27. (Original) An integrated circuit as described in claim 26, wherein the first and second sets of RF subcircuits are to operate during mutually exclusive time periods.

BEST AVAILABLE COPY

S/N 10/716,953

Page 5

CISCO-8481

28. (Original) An integrated circuit as described in claim 26, wherein the first and second sets comprise metal oxide semiconductor transistors.

29. (Original) An integrated circuit as described in claim 28, wherein the first and second sets comprise metal oxide semiconductor transistors in a CMOS configuration.

30-39. (Cancelled)

40. (Original) In a monolithic radio frequency (RF) integrated circuit, a method of providing bias current comprising:

partitioning at least part of the integrated circuit into a first set of one or more RF subcircuits and a second set of one or more RF subcircuits, such that the first set and second set operate in mutually exclusive time periods;

providing bias current to the first set of RF subcircuits, including switchably providing bias current to one or more RF subcircuits of the first set only for period of operation of the first set of RF subcircuits; and

providing bias current to the second set of RF subcircuits,

the switchably providing including controlling the rate of change of supplied bias current during the switching on or off of bias current.

41-46. (Cancelled)

BEST AVAILABLE COPY